

Design and implementation of an optimized multilevel power inverter structure based on C MEX and PSPICE

Mohammed Setti, Mohamed Cherkaoui

Engineering for Smart and Sustainable Systems Research Center, Mohammed V University in Rabat, Morocco

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ABSTRACT

In this paper, both symmetric and asymmetric operations for an optimized cascaded multilevel power inverter (MLI) are thoroughly examined. While symmetric configurations are more suitable for AC drives due to their equal power sharing among the various levels, the asymmetric topologies fulfill the higher number of power source combinations under the same power semiconductor switch count. Additionally, particular attention was put on the design of this optimized topology in terms of both reliability and power efficiency by managing redundant states and minimizing the number of power switch commutations. Furthermore, a fundamental switching frequency modulation (FSFM) is thoroughly described in C MEX programming language and then the resulting gating signals are fed into the power circuit designed with PSPICE. By applying this co-simulation approach, the control design task is greatly simplified while achieving advanced analyses with more realistic electronic devices.

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Corresponding Author:

Mohammed Setti,
Mohammadia School of Engineers,
Ibn-Sina Avenue, 765, Rabat, Morocco.
Email: mohammedsetti@research.emi.ac.ma

1. INTRODUCTION

Multilevel power inverters (MLIs) are considered as one of the most effective way to generate high quality AC power. Besides a good harmonic profile and low electromagnetic interferences that a staircase waveform can provide, some partial advantages related to design and reliability are directly obtained [1]. The power semiconductor switching devices in use can work in synergy to deliver the desirable power level, which let each one of them participate only in a fraction of the total power magnitude. Moreover, some multilevel power inverter structures can provide different switching combinations referred to as *redundant states* which can be useful to program fault-tolerant operations [2–5] monitored by switch fault diagnosis algorithms [6].

Despite of all their exciting advantages, MLI topologies come with a double-edged sword. They require a large number of power semiconductor valves which penalizes both the overall power system efficiency and reliability while meeting budget constraints [7]. The situation tends to be more gloomy with the introduction of dedicated ICs for driving power switches, so additional losses should be expected and the call for sophisticated controllers becomes inevitable. For all these reasons and more, several MLI topologies have been developed to address these shortcomings by limiting the number of their power switching devices [8–10].

In practice, the cascaded topologies with multiple DC sources are considered as one of the most authoritative multilevel topologies currently available, they have been successfully tested in some renewable

energy systems for more than a decade. They can be found either in symmetric or in asymmetric configuration depending on the magnitude of their voltage sources. Asymmetric nature of DC sources would provide extra levels to the output signals so as to enhance their harmonic profile.

However, in the most asymmetric structures, powers delivered by the various levels are quite different. This is a serious limitation of such configurations for applications in AC drives [11, 12]. Due to their nature, asymmetrical configurations have unequal power sharing; this doesn't allow the bridges to be easily replaced (as the high and low side bridges most likely to be made by different power devices) and hence lose the advantage of modularity [11]. Also, it goes without saying that the peak inverse voltage (PIV) is noticeably greater in asymmetric operation.

The next section deals with an optimized power inverter topology under asymmetric operation. It has already been the subject of a previous work [13], but nevertheless, did neither stress any aspect of power efficiency or reliability of such power converter nor try to address the issue of the PIV withstanding. For these reasons and more, this article was fully rewritten, better arranged and thoroughly upgraded all the simulation results. Also, a new symmetric configuration is proposed on the basis of what was fulfilled, where redundant states in different operating modes required by fault-tolerant applications are highlighted and commented. Afterwards, the power efficiency of the proposed MLI topology is evaluated and compared to some state-of-the-art topologies. Furthermore, a guide to co-simulating power control systems using C programming language *via* Simulink MEX S-function under PSPICE environment is newly provided. This will bring more advantages over conventional approach adopted in such previous work and avoid to manage the dizzy number of Simulink function blocks. The generated digital signals can be transferred to the target embedded system or fed into the power circuit made from realistic electrical components under PSPICE. Results and discussion are carried out while relevant conclusions are highlighted at the end of this paper.

2. PROPOSED POWER INVERTER TOPOLOGY

In contrast to some structures suggested in the literature that call for extra capacitors, diodes or transformers to clamp/bring the voltage up to a suitable level, the proposed MLI topology depicted in Figure 1(a) (top) makes use only of voltage sources and switches (the Schottky diode D_S only take part of the driving circuitry of Figure 1(a) (base) to allow asymmetric turn on and off). Namely, for the symmetric scheme (where $k = 1$), there are four unidirectional ($S_{1,j}$ to $S_{3,j}$) and two bidirectional ($S_{2,j}$) power switches supplied by two identical DC voltage sources. The same framework can be extended to provide asymmetric operation by having the voltage of the second DC source equals twice that of the first one ($k = 2$). Notice that $S_{1,1}$ and $S_{1,2}$ share a common drain while $S_{3,1}$ and $S_{3,2}$ share a common source electrode. On the other hand, asymmetric arrangement with $k = -3$ is also possible but require that the location between the pair of switches $S_{1,j}$ and $S_{2,j}$ then between $S_{2,j}$ and $S_{3,j}$ are swapped. This arrangement will not be considered here because it exhibits the same performance as that with $k = 2$.

The current path of different operating modes of the proposed topology is depicted by Figure 1(b) while a list of switch states is tabulated in Table 1. In order to ensure that all the desirable voltage levels are produced and every voltage source is protected against short-circuits. The general rule can be then defined as follows:

$$S_{i,j} = \{0, 1\} \left| \prod_{j=1}^2 \sum_{i=1}^3 S_{i,j} = 1. \right. \quad (1)$$

Since the proposed structure are built from unidirectional and bidirectional power switches, and because each topology comes with a number of redundant switching states, different switching scenarios are available. When one or more power switches within a given power inverter circuit fail, either permanently or temporarily, the power delivered to the load will therefore be altered and causing a decrease in the overall system reliability. To prevent that from happening, a fault-tolerant application should be programmed by making use of available redundant switch states. For each configuration, the Table 2 summarizes these redundant states and provides the switching patterns accordingly. Also, some hints are given to address the power consumption issue.

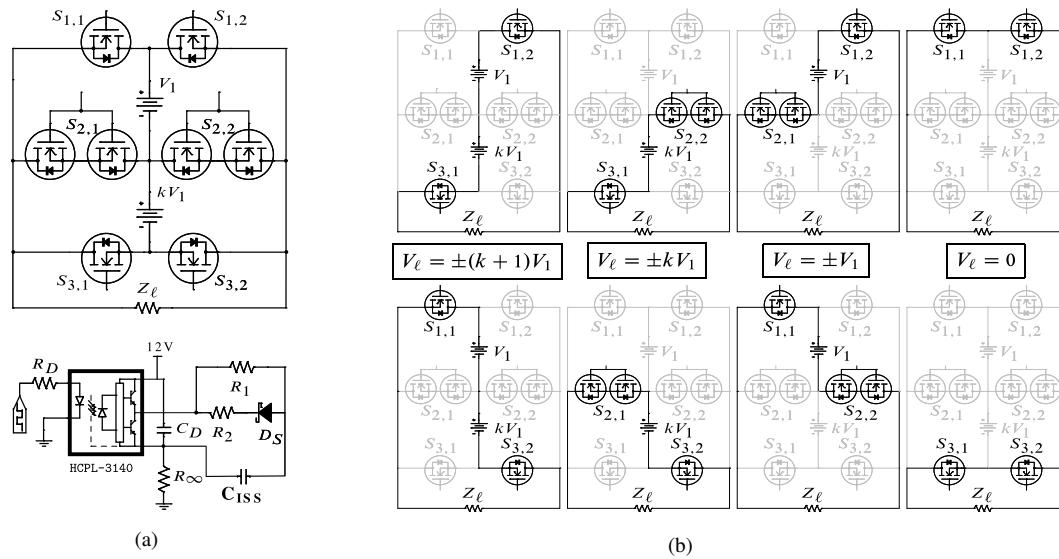


Figure 1. (a) Proposed power inverter structure (top) and optocoupler and totem-pole gate driver (base). (b) Current path of different operating modes under symmetric ($k = 1$) and asymmetric ($k = 2$) setups. k is the voltage ratio

Table 1. Switching combinations of the proposed MLI topology for symmetric and asymmetric operations

level in p.u.	symmetric						asymmetric					
	S _{1,1}	S _{1,2}	S _{2,1}	S _{2,2}	S _{3,1}	S _{3,2}	S _{1,1}	S _{1,2}	S _{2,1}	S _{2,2}	S _{3,1}	S _{3,2}
-3	n/a	n/a	n/a	n/a	n/a	n/a	0	1	0	0	1	0
-2	0	1	0	0	1	0	0	0	0	1	1	0
-1	0	1	1	0	0	0	0	1	1	0	0	0
-1 (redundant state)	0	0	0	1	1	0	n/a	n/a	n/a	n/a	n/a	n/a
0	1	1	0	0	0	0	1	1	0	0	0	0
0 (redundant state)	0	0	0	0	1	1	0	0	0	0	1	1
0 (redundant state)	0	0	1	1	0	0	0	0	1	1	0	0
1	1	0	0	1	0	0	1	0	0	1	0	0
1 (redundant state)	0	0	1	0	0	1	n/a	n/a	n/a	n/a	n/a	n/a
2	1	0	0	0	0	1	0	0	1	0	0	1
3	n/a	n/a	n/a	n/a	n/a	n/a	1	0	0	0	0	1

3. POWER EFFICIENCY COMPARISON WITH OTHER TOPOLOGIES

Mainly, there are two types of power losses dissipated within a semiconductor switching device, namely the conduction and the switching losses. The former losses are associated with the drain-to-source ON resistance, while the latter are linked up with the input/output parasitic capacitances C_{iss} and C_{oss} . Also and since all FETs are symmetrical devices, the average power conduction loss of the MOSFET is calculated as follows:

$$P_m = R_{ds(ON)} \frac{1}{2\pi} \int_0^{2\pi} i^2(t) dt = R_{ds(ON)} I_{RMS}^2, \quad (2)$$

Where $R_{ds(ON)}$ is the drain-to-source ON-state resistance of the power MOSFET. The average power conduction loss P_m can be evaluated to as the product of $R_{ds(ON)}$ and the square of the RMS drain current. Considering that at instant t , there are n MOSFETs in the current path, the average value of the conduction power loss P_c of the DC-to-AC converter can be formulated as below:

$$P_c = \frac{P_m}{2\pi} \int_0^{2\pi} n(t) dt = P_m N_{AVG}. \quad (3)$$

Table 2. Redundant switch states under symmetric and asymmetric operations of the proposed MLI

Configuration	Redundancy	State	Pattern	Note
Asymmetric ($k = 2$)	2	0	$S_{3,1} + S_{3,2}$	Preferred (low power losses)
		0	$S_{2,1} + S_{2,2}$	Not recommended (high power losses)
Symmetric ($k = 1$)	4	$-V_1$	$S_{2,2} + S_{3,1}$	Identical performance
		0	$S_{3,1} + S_{3,2}$	Suitable when either $-V_1$ or $+V_1$ redundant state is used (low switching power losses)
		0	$S_{2,1} + S_{2,2}$	Not recommended (high power losses)
		$+V_1$	$S_{2,1} + S_{3,2}$	Identical performance

The switching power loss P_s is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage [14]. This can be written as follows:

$$P_s = \left(\sum_{k=1}^n \sum_{i=1}^{n_{on,k}} E_{on,ki} + \sum_{k=1}^n \sum_{i=1}^{n_{off,k}} E_{off,ki} \right) f_{sw}, \quad (4)$$

where f_{sw} is the switching frequency and $n_{on,k}$ and $n_{off,k}$ are the number of turn-on and turn-off of the k th MOSFET during a fundamental cycle. Also, $E_{on,ki}$ is the energy loss of the k th MOSFET during the i th turn-on and $E_{off,ki}$ is the energy loss of the k th MOSFET during the i th turn-off. Since most MLI structures involve high number of power switches, the reason to drive them by fundamental frequency modulation (FSFM) becomes inevitable so as to alleviate the power switching losses, which makes the conduction losses ($R_{ds(ON)}$) dominate over those incurred by the switching transitions (Q_g and C_{oss}):

$$2R_{ds(ON)} I_{RMS}^2 \gg (Q_g V_{gs} + C_{oss} V_{ds}^2) f_{sw}, \quad (5)$$

where Q_g is the gate charge of the MOSFET, V_{gs} is the RMS gate-to-source voltage, C_{oss} is the MOSFET output parasitic capacitance ($C_{gd} + C_{ds}$) and V_{ds} is the RMS drain-to-source voltage. The total loss P_t is then the sum of the conduction and switching losses:

$$P_t = P_c + P_s \approx P_c. \quad (6)$$

Table 3. Total blocking voltage and active power switches in different cascaded MLI topologies under FSFM

Topology	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	Proposed
No. of DC sources	3	2	2	2	5	2	2	4	2
No. of bidirectional switches	0	0	1	6	1	2	0	2	2
No. of unidirectional switches	6	6	6	0	10	6	6	5	4
symmetric (5-level)									
No. of active power switches	<i>n/a</i>	24	28	32	<i>n/a</i>	28	<i>n/a</i>	26	20
Total blocking voltage in V_1	<i>n/a</i>	8	11	10	<i>n/a</i>	14	<i>n/a</i>	11	10
asymmetric (7-level)									
No. of active power switches	36	36	<i>n/a</i>	48	72	44	36	40	32
Total blocking voltage in V_1	18	12	<i>n/a</i>	16	18	22	12	16	16

Most power efficient topologies cannot be evaluated just in terms of how many electronic parts they would require, but in addition, they should be assessed with regard to the total number of their active power switches over one full-time period and their voltage blocking capability. As it was shown in Tables 3 and 4, the proposed MLI excels all the 8 structures depicted by Figure 2 both in terms of power efficiency η and total number of active power switches. The total blocking voltage comparison is also considered since switching devices' ratings are always correlated to their maximum blocking voltage. Moreover, the total harmonic distortion (THD) and individual power dissipation in every power switch are tabulated in Table 4. Finally, it should be pointed out that all the bidirectional switches are assumed to be arranged by two back-to-back N-channel power MOSFETs.

Table 4. Comparison of THD, switch power dissipation (in Watts) and power efficiency of selected highly efficient cascaded MLI topologies under FSFM

Topology	symmetric — 7.2% thd _i , 17.9% thd _v —								asymmetric — 4.0% thd _i , 12.5% thd _v —							
	$S_{1,1}$	$S_{1,2}$	$S_{2,1}$	$S_{2,2}$	$S_{3,1}$	$S_{3,2}$	Σ	η (%)	$S_{1,1}$	$S_{1,2}$	$S_{2,1}$	$S_{2,2}$	$S_{3,1}$	$S_{3,2}$	Σ	η (%)
(a)	n/a	n/a	n/a	n/a	n/a	n/a	—	—	.599	.590	.606	.588	.599	.593	3.57	99.66
(b)	.636	.651	.659	.663	.688	.684	3.98	99.63	.590	.601	.590	.598	.588	.604	3.57	99.66
(g)	n/a	n/a	n/a	n/a	n/a	n/a	—	—	.588	.601	.590	.604	.591	.601	3.58	99.66
Proposed	.630	.627	.258	.260	.485	.486	2.74	99.75	.448	.444	.396	.396	.554	.556	2.79	99.73

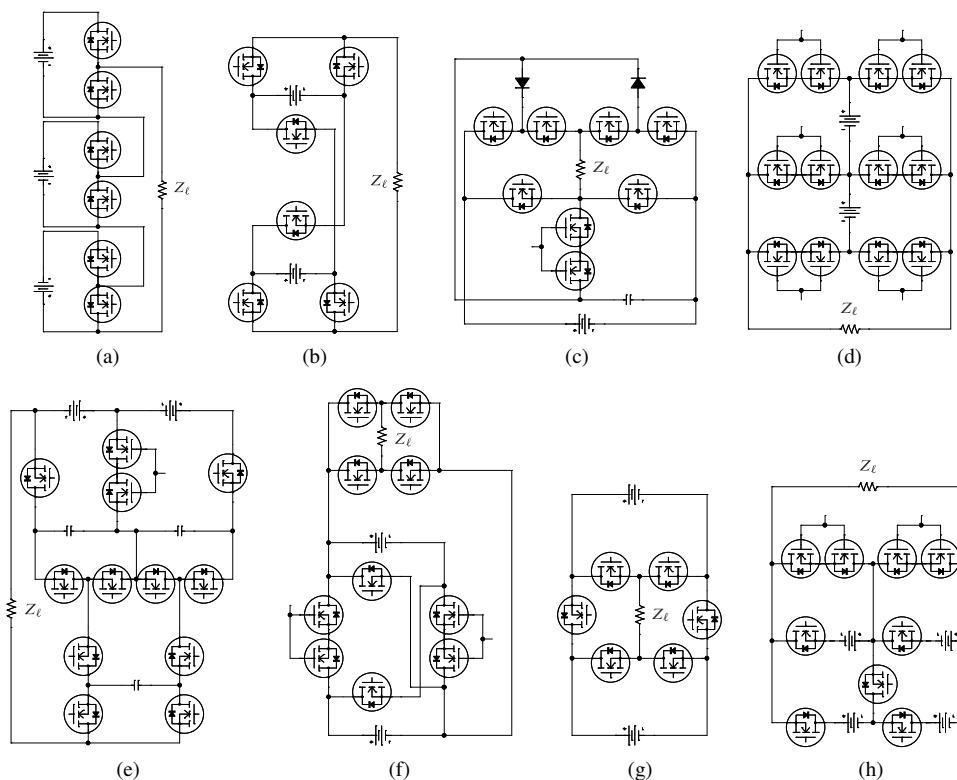


Figure 2. Cascaded MLI topologies with reduced power switch count presented in literature: (a) from [16], (b) from [17], (c) from [18], (d) from [19], (e) from [20], (f) from [21], (g) from [7] and (h) from [22]

4. C MEX AND PSPICE CO-SIMULATION

This section is devoted to co-simulate the proposed MLI using C MEX S-function and PSPICE program. Instead of using mathematical function blocks and graphically connecting them together to build system models, the user can rely on the system-functions called *C MEX S-functions*, which are defined as computer language description written in C/C++ programming language, to benefit from their capabilities to interact with the Simulink engine. Henceforth, this approach has the advantage to not be cumbersome as the former does and requires less hardware resources and time during execution and maintenance. However, only the switching control can be achieved that way, since Simulink uses only ideal models and non technology-specific devices. On the contrary to other simulation programs like Simscape Electrical, PLECS and PSIM, PSPICE is an industry standard SPICE-based simulator and is primarily intended to model technology-specific electronic components so that to provide in-depth details about some realistic circuit behaviors during simulation. For these reasons and more, the proposed MLI circuit is described by netlist.

C MEX S-functions are based on the C language. They must be compiled as MEX files using `mex` utility, so the resulting binary file is platform-dependent and dynamically loadable executable utilized by Simulink program [15]. Figure 3(a) depicts the typical workflow for C MEX compiling and integrating into Simulink models. During the simulation, the Simulink engine must retrieve information about the function used by the

C MEX S-function. As the simulation proceeds, the C MEX S-function, the Ordinary Differential Equations (ODE) Solver and the Simulink engine interact together to achieve specific tasks. The interaction between C MEX S-function and Simulink engine is realized by invoking callback methods that the S-function implements.

In order to model the gate switching patterns required to drive the proposed power inverter, the engine should invoke sequentially the C MEX S-function callback methods as illustrated in the flowchart of the Figure 3(b). The methods drawn in black line are mandatory, whereas those shown in gray color are optional. Also, in the flowchart given by the Figure 3b, mainly three steps are involved: (I) initialization, (II) calculation of switching outputs in the major time step, and (III) termination of the simulation. The `mdlInitializeSizes()` callback method aims to identify the width and data type of different input and output ports. The `mdlInitializeSampleTimes()` is then invoked to specify both the offset time and sample rate at which the S-function should operate.

Afterwards, at every simulation time step, the `mdlOutputs()` method is called to compute the S-function's switching outputs by means of the Simulink engine and then dispatches the results as array elements. The block's core logic has to be implemented inside the body of this callback method. The FSFM algorithm follows this requirement, which in fact corresponds to one of the switching pattern set tabulated in Table 1. As its name implies, the `mdlTerminate()` method is called to perform any tasks required at the end of the simulation process like closing debugging files or freeing dynamic memory allocations.

The generated FSFM gating signals for driving the proposed MLI are based on the NLC scheme [8] and given by Figure 4 under symmetric and asymmetric operations. The rounding functions defined inside `mdlOutputs()` must handle the misleading number representation of half-integers by defining a proper tie-breaking rule such as round-half-to-even. These signals can either be fed into PSPICE or directly sent to the target hardware *via* the Embedded Coder, which allows the code to be compiled and executed on any processor.

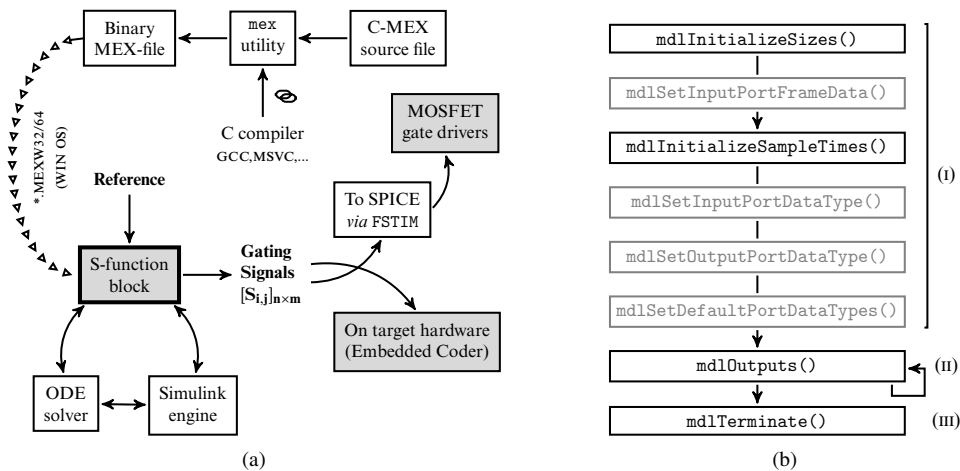


Figure 3. (a) Typical workflow for C MEX compiling and integrating into Simulink models. The results can be either linked to PSPICE or run on the target hardware *via* the Embedded Coder. (b) C MEX S-function callback methods flowchart used for modeling the switching controller

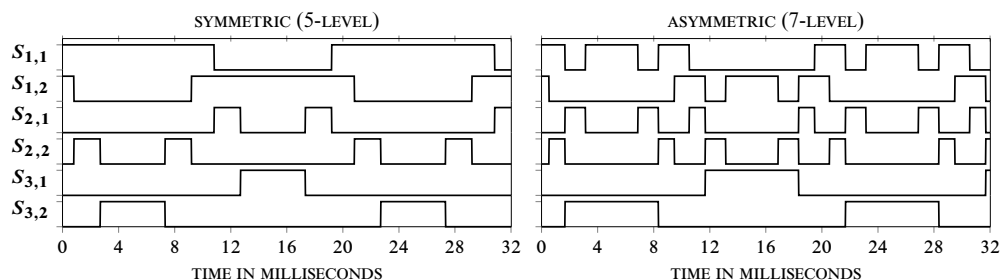


Figure 4. Gating signals for the proposed MLI for both symmetric and asymmetric configurations under FSFM

The PSPICE file stimulus (FSTIM) devices are aimed to provide digital signals to a given circuit node through external data file [23], so as to provide a link to the FSFM gating signals. Another approach called PSPICE SLPS interface has already been suggested to provide co-simulation under Simulink [24]. This tool comes with good features, but still remain some drawbacks that should be addressed:

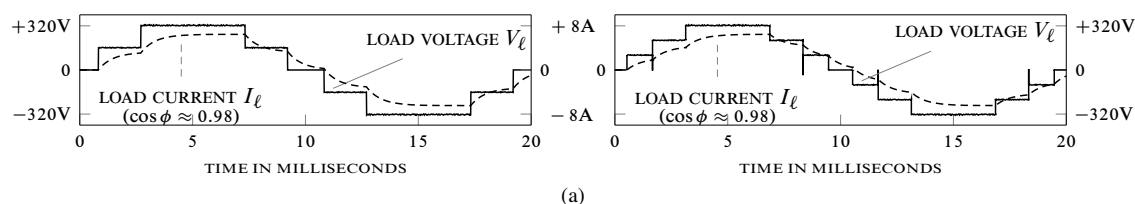
- The actual electronic block is substituted with an *ideal model* since the simulation of the power circuit is set up under Simulink environment;
- The internal properties of PSPICE that have smaller time steps than those of Simulink cannot be checked. Also, some Simulink minor steps are skipped, and thus data is not fully exchanged with PSPICE [25];
- The SLPS data exchange is synchronized with Simulink steps. To prevent overlooking phenomena from happening, Simulink maximum step size should be chosen carefully, so to ensure the best trade-off between accuracy and simulation time;
- Only one SLPS block per Simulink model is allowed [25]. The number of interfaces an SLPS block can handle is limited. As reported by many users, Simulink will crash once the limit is exceeded;
- Some limitations are inherited from the fact that Simulink are generic simulation programs not targeted for mixed-signal electronic designs.

In contrast to how the SLPS interface tool operates, the suggested co-simulation approach is now fulfilled thoroughly under PSPICE environment, so as to prevent the idealization of the used electronic devices. Consequently, the overlooking and data exchange issue are no longer a problem as soon as the gating signals retrieved from Simulink are correctly processed and adapted to the requirements of PSPICE stimulus devices.

The driving of the different power MOSFETs of Figure 1(a) (top) is done by the Avago HCPL-3140 optocoupler based drivers shown by Figure 1(a) (base). However, each non-inverting optically isolated totem-pole gate driver requires one floating power supply of 12 volts with respect to the ground node V_{EE} , so as to be able to drive high-side N-channel power MOSFETs. Additionally, a 100 nF bypass capacitor C_D must be added to stabilize the operation of the high gain linear amplifier, otherwise, the switching functionality may be compromised. Finally, PSPICE simulator needs at least one ground or *node zero* to reference all the calculated voltages, so in order to isolate the control side of the circuit from the power side and distinguish between the two side grounds, a resistance R_∞ with high value is used to prevent floating node error from happening. Moreover, the load Z_ℓ represents an inductive load with a DPF = 98 % lagging formed by an $R_\ell = 50 \Omega$ in series with an $L_\ell = 32 \text{ mH}$.

All the power MOSFETs operate at fundamental frequency (50 Hz) and are under hard switching condition. Low switching power losses are always correlated with fast commutations which are the major reason for electromagnetic interference and voltage spike across the drain and source terminals due to the existence of stray inductances. Additionally, the switching speed varies with respect to the value of the gate resistor R_G which would make the selection more difficult in order to avoid the overlap time that will cause large current surge.

Both Figures 5(d) and 5(e) present some surges in the drain current of the MOSFETs on each column when the external gate resistors R_2 and the Schottky diodes D_S are omitted from the driving circuit of Figure 1(a)(base). As it can be seen, the maximum rating allowed for the pulsed drain current is exceeded in case of a 600V CoolMOS CFD7 N-channel power MOSFET, so in order to get rid from this situation, each power switch should be driven through different gate resistors to allow asymmetric turn on and turn off. Figure 5(f) and 5(g) highlight, respectively, the difference by plotting the gate-to-source voltage V_{GS} for both $S_{2,2}/S_{3,2}$ $S_{1,1}/S_{2,1}$ that have been equipped with gate resistors on top of those which have no additional gate resistors. As the Figures 5(h) and 5(i) suggest, the drain current spikes through the six power switches are now mostly vanished. The AC output voltage and current of the proposed 5- and 7-level power inverters are illustrated together through the Figure 5(a) under an inductive load with a DPF ≈ 0.98 lagging. Additionally, the voltage/current harmonic profiles for both configurations are also included, respectively, by Figures 5(b) and by Figures 5(c), wherein their THD are calculated separately within one complete time period (20 ms).



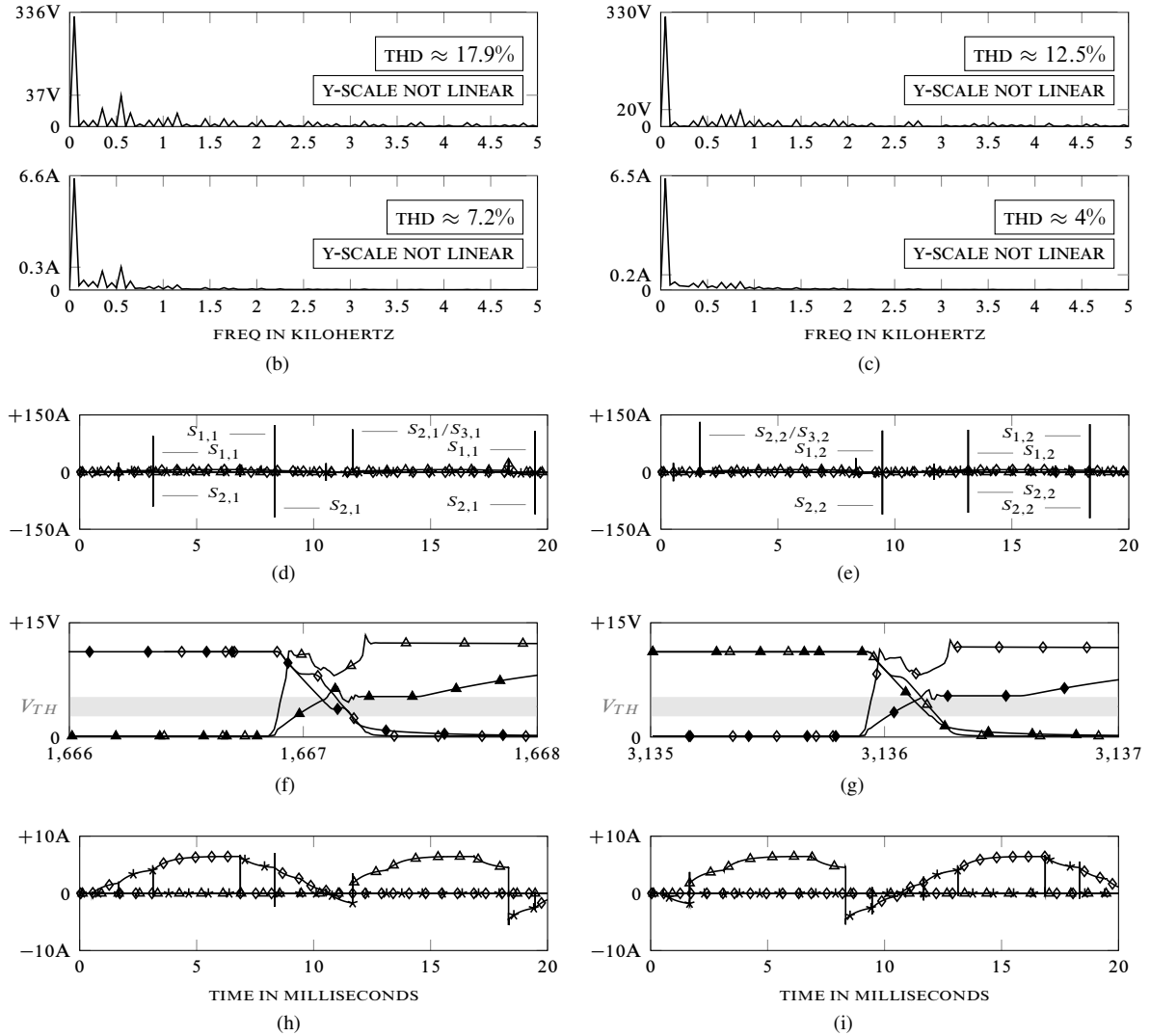


Figure 5. Output waveforms/spectra and switching characteristics of the proposed MLI with an inductive load ($\text{DPF} \approx 0.98$). (a) Load voltage V_ℓ and current I_ℓ waveforms in symmetric/asymmetric configuration, respectively. (b) Load voltage/current spectrum under symmetric setup. (c) Load voltage/current spectrum under asymmetric setup (The y-axis scale of fundamental spectrum and harmonic spectra is nonlinear). Drain current through the power MOSFETs where no gate resistor ($R_2 = 0 \Omega$): (d) $S_{1,1}$ (\diamond), $S_{2,1}$ (\star) and $S_{3,1}$ (\triangle). (e) $S_{1,2}$ (\diamond), $S_{2,2}$ (\star) and $S_{3,2}$ (\triangle). Voltage across the gate and source terminals of the power MOSFETs: (f) $S_{2,2}$ (\diamond and \star) and $S_{3,2}$ (\triangle and \star) with/without gate resistors. (g) $S_{1,1}$ (\diamond and \star) and $S_{2,1}$ (\triangle and \star) with/without gate resistors (V_{TH} is the gate threshold voltage of the 600V CoolMOS CFD7 power MOSFET). Drain current when gate resistors and Schottky diodes are added: (h) $S_{1,1}$ (\diamond), $S_{2,1}$ (\star) and $S_{3,1}$ (\triangle). (i) $S_{1,2}$ (\diamond), $S_{2,2}$ (\star) and $S_{3,2}$ (\triangle)

5. CONCLUSION

In this article, the symmetric and asymmetric configurations of the proposed MLI were compared to some well-established topologies in the literature. It has shown that the proposed structure accomplishes the highest power efficiency score ($\eta \approx 99.73 - 99.75\%$) by restraining the number of active power switches per cycle. Moreover, the proposed symmetric topology exhibits low total blocking voltage and several redundant switch states, which would bring additional enhancement to the overall system reliability. Alternatively, asymmetric structure provides a good harmonic profile (about 4% THD_i and 12.5% THD_v) which positively impact the AC side low-pass filter in order to comply with the international standards in terms of power quality.

Afterwards, the FSFM was described in C MEX and run through a single Simulink S-function block. This would bring significant enhancement in development and simulation speed and make maintenance effortless when compared to the conventional approach based on graphical modeling. The generated gating signals can be either sent to the embedded hardware or integrated as digital stimuli through the PSPICE file stimulus device. This technique has some advantages over the SLPS interface tool especially when simulating open-loop SMPS topologies and make use of more realistic electronic devices provided by almost every electronics manufacturers.

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